I. Amendments to the Claims

This listing of claims replaces without prejudice all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-4 (Cancelled).

5. (Currently Amended) A feed-forward amplifier, comprising:

an amplifier portion including a main signal path, a feed-forward signal path, a signal cancellation loop, and an intermodulation cancellation loop; [[,]] and

a detector-controller portion including a signal-power detector/processor, and a switch,

wherein the switch ~~is operable~~ operates (i) on start-up to ~~connect~~ couple the signal-power detector/processor to the signal cancellation loop so that it ~~is operable to~~ balances the signal cancellation loop so as to minimize signal power in the feed-forward signal path, and (ii) thereafter ~~is connected~~ operates to couple the signal-power detector/processor to the main signal path downstream of the intermodulation cancellation loop so as to operate the signal cancellation loop to minimize intermodulation in the main signal path downstream of the intermodulation cancellation loop.

6. (Currently Amended) The feed-forward amplifier of claim 5, wherein the main signal path includes:

an input port;

an output port;

a first main path splitter, an input of which is connected to the input port so that when an input signal applied to the input port it is split by the first main path splitter into a main signal and a feed-forward signal;

a main signal path gain and phase adjuster, an input of which is connected to a first output of the first main path splitter, the main signal path gain and phase adjuster having a gain-control input tap T_1 and a phase-control input tap T_2 configured so that the voltage levels on the taps control the gain and phase of the main signal;

a main amplifier, an input of which is connected to the output of the main signal path gain and phase adjuster;

a second main path splitter, an input of which is connected to an output of the main amplifier;

a main signal path delay element, an input of which is connected to a first output of the second main path splitter; [[,]]

a first main path coupler, a first input of which is connected to an output of the main signal path delay element; and

a third main path splitter, an input of which is

connected to an output of the first main path coupler and a first output of which is connected to the output port and a second output of which is connected to an input of an intermodulation receiver,

wherein the feed-forward signal path includes:

a feed-forward signal path delay element, an input of which is connected to a second output of the first main path splitter, the delay imposed by the feed-forward signal path delay element selected to approximately match the delay in the main signal caused by the main amplifier;

a feed-forward path coupler, a first input of which is connected to an output of the feed-forward signal path delay element and a second input of which is connected to an attenuator connected to a second output of the second main path splitter, the attenuation selected so that the undistorted portion of the main signal provided to the feed-forward path coupler is approximately cancelled out by the feed-forward signal;

a feed-forward path splitter, an input of which is connected to an output of the feed-forward path coupler;

a feed-forward signal path gain and phase adjuster, an input of which is connected to a first output of the feed-forward path splitter, the feed-forward signal path gain and phase adjuster having a gain-control input tap T_3 and a phase-control input tap T_4; and

a correctional amplifier, an input of which is connected to the output of the feed-forward signal path gain and phase adjuster and an output of which is connected to a second input of the first main path coupler,

wherein the delay in the correctional amplifier is approximately equal to the delay added by the main signal path delay element, and

wherein the detector-controller portion includes:

the switch, which comprises ~~is~~ a SPDT switch, the first throw of which is connected to an output of the intermodulation receiver and the second throw of which is connected to a second output of feed-forward signal path gain and phase adjuster;

the signal-power detector/processor, an input of which is connected to the pole of the SPDT switch, the signal-power detector/processor configured to extract and process data from the signal presented to its input indicating how to steer the gain-control input tap T_1 and the phase-control input tap T_2 to minimize the signal presented to its input;

a signal-power gain controller, an input of which is connected to a first output of the signal-power detector/processor, the signal-power gain controller configured to steer the gain-control input tap T_1 in response to data provided by the signal-power detector/processor to minimize signal power at the feed-forward path splitter when

the SPDT switch is set to connect the input of the signal-power detector/processor to the second output of the feed-forward path splitter and to minimize the intermodulation received by the intermodulation receiver when the SPDT switch is set to connect the input of the signal-power detector/processor to the output of the intermodulation receiver;

a signal-power phase controller, an input of which is connected to a second output of the signal-power detector/processor, the signal-power phase controller configured to steer the phase-control input tap T_2 in response to data provided by the signal-power detector/processor to minimize signal power at the feed-forward path splitter when the SPDT switch is set to connect the input of the signal-power detector/processor to the second output of the feed-forward path splitter and to minimize the intermodulation received by the intermodulation receiver when the SPDT switch is set to connect the input of the signal-power detector/processor to the output of the intermodulation receiver;

an intermodulation detector/processor, an input of which is connected to the output of the intermodulation receiver, the intermodulation detector/processor configured to extract and process data from the signal presented to its input indicating how to steer the gain-control input tap T_3 and the phase-control input tap T_4 to minimize the signal

presented to its input;

an intermodulation gain controller, an input of which is connected to a first output of the intermodulation detector/processor and which steers the gain-control input tap T_3 in response to data provided the intermodulation detector/processor to minimize intermodulation received by the intermodulation receiver; and

an intermodulation phase controller, an input of which is connected to a second output of the intermodulation detector/processor and which steers the phase-control input tap T_4 in response to data provided the intermodulation detector/processor to minimize intermodulation received by the intermodulation receiver,

wherein, upon startup of the feed-forward amplifier, the SPDT switch is set so as to connect the feed-forward path splitter to the signal-power detector/processor until the total power in the feed-forward path and the intermodulation received by the intermodulation receiver are minimized, and then set so as to connect the intermodulation receiver to the signal-power detector/processor.

7. (Currently Amended) A method for operating a feed-forward amplifier having a signal cancellation loop and a intermodulation cancellation loop, comprising:

on startup, operating the feed-forward amplifier so that the signal cancellation loop is balanced so as to

minimize signal power in ~~its~~ the feed-forward amplifier's feed-forward path while the intermodulation cancellation loop is operated so as to minimize intermodulation at the feed-forward amplifier's output; and

then, when signal power in the feed-forward path and intermodulation at the feed-forward amplifier's output have both been minimized, operating the ~~feed-forward amplifier~~ signal cancellation loop so as to minimize intermodulation at ~~its~~ the feed-forward amplifier's output while continuing to operate the intermodulation cancellation loop so as to minimize intermodulation at feed-forward amplifier's output.

8. (Currently Amended) A method for operating a feed-forward amplifier having a signal cancellation loop including a first gain and phase adjuster[[,]] and a main amplifier forming a portion of [[a]] the feed-forward amplifier's main signal path, ~~and a feed-forward signal path output for providing a feed-forward signal,~~ and an intermodulation cancellation loop ~~connected to the feed-forward signal path output~~, including a second gain and phase adjuster, a correctional amplifier, and a correctional coupler for coupling the output of the correctional amplifier to the main signal path downstream of the main amplifier, the method comprising:

steering the first gain and phase adjuster so as to

minimize signal power ~~at~~ in the feed-forward amplifier's feed-forward signal path ~~output~~ and the second gain and phase adjuster so as to minimize intermodulation downstream of the correctional coupler; and

then, when the signal power ~~at~~ in the feed-forward signal path ~~output~~ and the intermodulation downstream of the correctional coupler have both reach minimums, steering both of the gain and phase adjusters so as to minimize the intermodulation downstream of the correctional coupler.

9. (New) The feed-forward amplifier of claim 5, wherein the amplifier portion has an input port and an output port and includes:

the main signal path connecting the input port to the output port and including a gain and phase adjuster, the main amplifier, and a delay element downstream of the main amplifier and the gain and phase adjuster; and

the feed-forward signal path having an input connected to the input port, an output coupled to the main signal path at a coupler between the delay element and the output port, a delay element, a gain and phase adjuster, and a correctional amplifier;

an intermodulation receiver coupled to the main signal path at a path splitter between the coupler at the output of the feed-forward signal path and the output port; and

an attenuator coupled to the main signal path at a path splitter that is downstream of the main amplifier and the gain and phase adjuster and upstream of the delay element and coupled to the feed-forward signal path at a coupler that is downstream of the delay element and upstream of the gain and phase adjuster and the correctional amplifier; and

the detector-controller portion includes: the signal-power detector/processor, an output of which is connected to the gain and phase adjuster in the main signal path so that the signal-power detector/processor controls the gain and phase of a main signal amplified in the main signal path; and

an intermodulation detector/processor, an input of which is connected to the intermodulation receiver and an output of which is connected to the gain and phase adjuster in the feed-forward signal path so that the intermodulation detector/processor controls the gain and phase of the feed-forward signal so as to minimize intermodulation at the output port of the feed-forward amplifier;

wherein the detector-controller portion also includes a switch which on start-up of the feed-forward amplifier connects an input of the signal-power detector/processor to the feed-forward signal path at a splitter downstream of the coupler of the attenuator to the feed-forward signal path and upstream of the gain and phase adjuster and the correctional amplifier so that the signal-

power detector/processor controls the gain and phase of the main signal so as to minimize signal power in the feed-forward signal path and then, after signal power in the feed-forward signal path and intermodulation at the output port have both been minimized, disconnects the input of the signal-power detector/processor from the feed-forward signal path and connects the input of the signal-power detector/processor to the intermodulation receiver so that the signal-power detector/processor controls the gain and phase of the main signal so as to minimize intermodulation at the output port of the feed-forward amplifier.